

October 15-19, 2016



#### General Co-Chairs

Wei-Chung Hsu, Natl. Taiwan U.  
Chia-Lin Yang, Natl. Taiwan U.

#### Program Co-Chairs

Mikko Lipasti, Univ. Wisconsin  
Hsien-Hsin Lee, TSMC

#### Tutorial and Workshops Chair

David Brooks, Harvard

#### Local Arrangements

Shiao-Li Charles Tsao, NCTU  
Pi-Cheng Hsiu, Academia Sinica

#### Publication Chair

Bo-Cheng Charles Lai, NCTU

#### Publicity Co-Chairs

Koji Inoue, Kyushu Univ.  
Vijay Janapa Reddi, UT Austin  
Albert Cohen, INRIA

#### Finance Co-Chairs

Antonia Zhai, U. of Minnesota  
Yi-Jung Chen, NCNU

#### Web Chair

Hung-Wei Tseng, UC San Diego

#### Submission Chair

Chih-Chen Kao, Natl. Taiwan U.

#### Registration Chair

Ren-Shuo Liu, NTHU

#### Industrial liaison

Tien-Fu Chen, NCTU  
Mu-Tien Chang, Samsung USA  
Dongrui Fan, ICT

#### Travel Award Chair

Carole-Jean Wu, ASU

#### Steering Committee

Richard Belgard, Consultant, Chair  
David Albonese, Cornell  
Tom Conte, Georgia Tech  
Kemal Ebcioğlu, Global Supercomputing  
Matthew Farrens, UC Davis  
Scott Mahlke, Univ. of Michigan  
Bill Mangione-Smith, Consultant  
Onur Mutlu, CMU  
Yale Patt, UT Austin  
Milos Prvulovic, Georgia Tech  
Moinuddin Qureshi, Georgia Tech.

## The 49th Annual IEEE/ACM International Symposium on Microarchitecture

Co-sponsored by IEEE-CS TC-uARCH  and ACM SIGMICRO 

The International Symposium on Microarchitecture (MICRO) is the premier forum for the presentation and discussion of *new ideas* in microarchitecture, compilers, hardware/software interfaces, and design of advanced computing and communication systems. The goal of MICRO is to bring together researchers in the fields of microarchitecture, compilers, and systems for technical exchange. The MICRO community has enjoyed having close interaction between academic researchers and industrial designers -- we aim to continue and strengthen this longstanding tradition at the 49<sup>th</sup> MICRO in Taipei, Taiwan.

We invite original paper submissions on related to but not limited to the following:

- Processor, memory, interconnect, and storage architectures
- Hardware, software, and hybrid techniques for improving system performance, energy-efficiency, cost, complexity, predictability, quality of service, reliability, dependability, security, scalability, programmer productivity, etc.
- Processor, memory, storage, interconnect designs
- Architectures for instruction-level, thread-level, and memory-level parallelism: superscalar, VLIW, data-parallel, multithreaded, multicore, manycore, etc.
- Compiler and microarchitectural techniques for parallelism (ILP, TLP, MLP)
- Low-power, high-performance, and cost/complexity-efficient architectures
- Architectures for emerging platforms, including smartphones, tablets, cloud/datacenter, etc.
- Architectures and compilers for embedded processors, DSPs, GPUs, ASIPs (network processors, multimedia, wireless, etc.)
- Advanced software/hardware speculation and prediction schemes
- Microarchitecture techniques to better support system software, programming languages, programmability, and compilation
- Microarchitecture modeling and simulation methodology
- Insightful experimental and comparative evaluation and analysis of existing microarchitectures, hardware/software mechanisms and workloads

#### Important dates:

Abstracts due : **April 3<sup>rd</sup>, 2016**  
Papers due : **April 10<sup>th</sup>, 2016**  
Rebuttal period : **June 6<sup>th</sup> - June 10<sup>th</sup>, 2016**  
Notifications : **June 25<sup>th</sup>, 2016**

Submissions should follow the guidelines and formatting rules specified on the conference website. Papers that violate these guidelines and rules may be returned to author(s) without review.

<http://www.microarch.org/micro49/>