Call for Papers

The 51st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)

The International Symposium on Microarchitecture (MICRO) is the premier forum for the presentation and discussion of new ideas in microarchitecture, compilers, hardware/software interfaces, and design of advanced computing and communication systems. The goal of MICRO is to bring together researchers in the fields of microarchitecture, compilers, and systems for technical exchange. The MICRO community has enjoyed having close interaction between academic researchers and industrial designers—we aim to continue and strengthen this longstanding tradition at the 51st MICRO in Fukuoka, Japan.

Important Dates

Abstract	March 30th, 2018 at 11:59pm EDT
Full Paper	April 6th, 2018 at 11:59pm EDT
Rebuttal and Response	June 27th – July 3rd 2018
Notification	July 18th, 2018

We invite original paper submissions related to (but not limited to) the following topics:

- Processor, memory, interconnect, and storage architectures.
- Microarchitecture and compiler techniques for optimizing the memory hierarchy, analysis of new memory hierarchies, emerging architectures based on new memory technologies.
- Hardware, software, and hybrid techniques for improving system performance, energy-efficiency, cost, complexity, predictability, quality of service, reliability, dependability, security, scalability, programmer productivity, etc.
- Architectures for instruction-level, thread-level, and memory-level parallelism: superscalar, VLIW, data-parallel, multithreaded, multicore, many-core, etc.
- Architectures for emerging application domains such as deep learning, machine learning, relational computation, neuromorphic, quantum, etc.
- Accelerator designs and heterogeneous architectures including system-on-chip architectures, application specific fixed function, programmable, near-data and in-memory accelerators, etc.
- Compiler and microarchitectural techniques for parallelism (ILP, TLP, MLP).
- Compiler optimizations and microarchitecture techniques for heterogeneous architectures including CPU+GPUs, GPUs, SoCs, and programmable accelerators.
- Microarchitecture techniques to better support system software, programming languages, programmability, and compilation.
- Architectures and compilers for embedded processors, DSPs, GPUs, ASIPs (network processors, multimedia, wireless, etc.).
- Low-power, high-performance, and cost/complexity-efficient architectures.
- Architectures for emerging embedded platforms, including smartphones, automotive, server/cloud, etc.
- Advanced software/hardware speculation and prediction schemes.
- Microarchitecture modeling and simulation methodology.

- Insightful experimental and comparative evaluation and analysis of existing microarchitectures, hardware/software mechanisms and workloads.

Submissions should follow the guidelines and formatting rules specified on the conference website. Papers that violate these guidelines and rules may be returned to author(s) without review.